Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. The following listing provides the amended claims with deleted material crossed out and new material underlined to show the changes made.

Listing of Claims:

Claims 1-26. (Previously Canceled)

27. (Currently Amended) A method of routing a set of nets within a region of an integrated-circuit ("IC") layout, wherein each net within the set has a set of routable elements, the method comprising:

a) using a first set of lines to partition the IC region into a plurality of sub-regions;

b) defining at least one particular route for each particular net in the set, wherein each particular route for each particular net traverses the set of sub-regions that contain the set of routable elements of the particular net; and

~~b)~~c) using a second set of lines to measure congestion of routes for the nets within the IC region, wherein at least ~~some~~ a plurality of the lines in the second set are different from the lines in the first set.

28. (Original) The method of claim 27, wherein the first set of lines forms a first set of grids, and the second set of lines forms a second set of grids.

29. (Original) The method of claim 27, wherein the second set of lines includes intersecting diagonal lines that form a diagonal grid.

30. (Original) The method of claim 29, wherein the first set of lines includes intersecting horizontal and vertical lines that form a first rectilinear grid.

31. (Original) The method of claim 30, wherein the second set of lines further includes intersecting horizontal and vertical lines that form a second rectilinear grid.

32. (Original) The method of claim 31 further comprising:

using the second rectilinear grid to measure the congestion of routes in Manhattan directions;

using the diagonal grid to measure the congestion of routes in the diagonal directions.

33. (Original) The method of claim 31, wherein the second rectilinear grid is identical to the first rectilinear grid.

34. (Original) The method of claim 30, wherein the diagonal lines intersect at the center of the sub-regions created by the first set of lines.

35. (Currently Amended) A method of routing a set of nets within a region of an integrated-circuit ("IC") layout, wherein each net in the set has a set of routable elements, the method comprising:

a) partitioning the IC region into a plurality of sub-regions by using a first set of lines, wherein a plurality of diagonal routing paths exist between the sub-regions;

b) identifying the capacity of diagonal routing paths based on a second set of lines, wherein at least ~~some~~ a plurality of the lines in the second set are different from the lines in the first set; and

c) using the identified capacities to define routes for the set of nets, wherein a particular route for a particular net traverses the set of sub-regions that contain the set of routable elements of the particular net.

36. (Original) The method of claim 35, wherein the second set of lines includes diagonal lines.

37. (Original) The method of claim 36, wherein the diagonal lines are at an angle of +A° or -A° with respect to one of the axis of the IC region, wherein A is not 0 or 90, wherein the method uses the diagonal lines to identify the capacity of routing paths in ±A° directions between the sub-regions.

38. (Original) The method of claim 37, wherein A is 45.

39. (Original) The method of claim 37,

wherein the diagonal lines define a plurality of diagonal edges,

wherein each particular routing path intersects a particular diagonal edge,

wherein identifying the capacity of the diagonal routing paths comprises deriving each particular diagonal routing path's capacity from the size of the particular diagonal edge intersected by the particular diagonal routing path.

40. (Original) The method of claim 35, wherein each routing path is defined with respect to a particular wiring layer and each layer has a particular pitch, wherein identifying the capacity of the diagonal routing paths further comprises using the pitch of each particular routing path's layer to derive the particular routing path's capacity.

41. (Original) The method of claim 40 further comprising:

hierarchically partitioning the region into smaller and smaller sub-regions;

specifying a route for each net at each level of the hierarchy,

wherein the sub-regions at the lowest level of the hierarchy are Gcells,

wherein identifying the capacity of the diagonal routing paths at non-Gcell levels further comprises deriving the capacity of each particular diagonal routing path at non-Gcell levels from the number of tracks of wiring at the Gcell level in the direction of the particular routing path.

42. (Currently Amended) A method of ~~performing~~ routing a net in a layout, the net having a set of routable elements, the method comprising:

a) receiving a particular region of an integrated circuit ("IC") layout,

b) partitioning said region into a plurality of sub-regions,

wherein a plurality of diagonal and non-diagonal routing paths exist between said sub-regions,

wherein the diagonal routing paths are defined with respect to a first grid, and the non-diagonal routing paths are defined with respect to a second grid; and

c) for the net, using at least one diagonal routing path and at least one non-diagonal routing path to define and store a route that connects the set of sub-regions that contain the set of routable elements of the net.

43. (Original) The method of claim 42, wherein each routing path has a particular capacity, the method further comprising:

a) calculating the capacity of each particular diagonal routing path; and

b) calculating the capacity of each particular non-diagonal routing path.

44. (Original) The method of claim 43, wherein the capacity of the diagonal routing paths differ from the capacity of the non-diagonal routing paths.

45. (Currently Amended) The method of claim 43,

wherein the first grid includes a plurality of diagonal edges and the second grid includes a plurality of non-diagonal edges,

wherein each particular diagonal routing path intersects a particular diagonal edge, and each particular non-diagonal routing path intersect a particular non-diagonal edge,

wherein calculating each particular diagonal routing path's capacity comprises deriving the particular diagonal routing path's capacity from the size of the path's corresponding diagonal edge,

wherein calculating each particular non-diagonal routing path's capacity comprises deriving the particular's non-diagonal routing path's capacity from the size of the path's corresponding non-diagonal edge.

46. (Original) The method of claim 45, wherein the sizes of the diagonal and non-diagonal edges differ.

47. (Original) The method of claim 45, wherein each particular diagonal edge connects the centers of a particular pair of sub-regions that are diagonally aligned with respect to each other.

48. (Original) The method of claim 45,

wherein said IC layout includes a plurality of interconnect-line layers, each layer having a particular pitch value,

wherein each particular routing path is on a particular one of said layers,

wherein calculating the capacity of each particular diagonal routing path comprises dividing the size of the diagonal edge intersected by the particular diagonal routing path by the pitch value of the path's layer,

wherein calculating the capacity of each particular non-diagonal routing path comprises dividing the size of the non-diagonal edge intersected by the particular non-diagonal routing path by the pitch value of the path's layer.

49. (Currently Amended) A method of routing a set of pins, within a particular region of an integrated circuit ("IC") layout, according to an octagonal wiring model, the method comprising:

a) receiving the particular region of an integrated circuit ("IC") layout,

b) partitioning said region into a plurality of four-sided sub-regions, wherein a plurality of ±45° diagonal and Manhattan routing paths exist between said sub-regions, wherein the Manhattan routing paths are defined with respect to a first grid, and the ±45° diagonal routing paths are defined with respect to a second grid that is at 45° with respect to the first grid; and

c) using the diagonal and Manhattan routing paths to define and store a route that connects the set of sub-regions that contain the set of pins.

50. (Currently Amended) A computer readable medium comprising a computer program having executable code, the computer program for routing a set of nets within a region of an integrated-circuit ("IC") layout, wherein each net in the set has a set of routable elements, the computer program comprising:

a) a first set of instructions for partitioning the IC region into a plurality of sub-regions by using a first set of lines, wherein a plurality of diagonal routing paths exist between the sub-regions;

b) a second set of instructions for identifying the capacity of diagonal routing paths based on a second set of lines, wherein at least ~~some~~ a plurality of the lines in the second set are different from the lines in the first set; and

c) a third set of instructions for using the identified capacities to define routes for the set of nets, wherein a particular route for a particular net traverses the set of sub-regions that contain the set of routable elements of the particular net.

51. (Original) The computer readable medium of claim 50, wherein the second set of lines includes diagonal lines.

52. (Original) The computer readable medium of claim 51, wherein the diagonal lines are at an angle of +A° or -A° with respect to one of the axis of the IC region, wherein A is not 0 or 90, wherein the second set of instructions uses the diagonal lines to identify the capacity of routing paths in ±A° directions between the sub-regions.

53. (Original) The computer readable medium of claim 52,

wherein the diagonal lines define a plurality of diagonal edges,

wherein each particular routing path intersects a particular diagonal edge,

wherein the second set of instructions derives each particular diagonal routing path's capacity from the size of the particular diagonal edge intersected by the particular diagonal routing path.

54. (Original) The computer readable medium of claim 53,

wherein each routing path is defined with respect to a particular wiring layer and each layer has a particular pitch,

wherein the second set of instructions further derives the capacity of each particular diagonal routing path from the pitch of the particular routing path's layer.

55. (Currently Amended) The ~~method~~ computer readable medium of claim 54 further comprising:

a) third set of instructions for hierarchically partitioning the region into smaller and smaller sub-regions;

b) fourth set of instructions for specifying a route for each net at each level of the hierarchy,

wherein the sub-regions at the lowest level of the hierarchy are Gcells,

wherein the second set of instructions further derives the capacity of each particular diagonal routing path at non-Gcell levels from the number of tracks of wiring at the Gcell level in the direction of the particular routing path.